Second Embodiment

FIG. 11 is a view showing a configuration of overall integrated circuit chip using the hybrid standard cell architecture according to a second embodiment of the present invention. The second embodiment of the present invention is concerned with a large scale circuit system, in which memories. CPU core, ALU, A/D converter, D/A converter, display, and various I/O circuits are included. In the large scale circuit system such as recent LSIs for multimedia application, miscellaneous subsystems are mounted with logic circuit on a same LSI chip, and the second embodiment of the present invention explain the large scale circuit system. More particularly, an LSI will be explained wherein megacells 213 such as ROM, RAM, etc., megafunctions 211, 212 such as ALU, CPU, core, etc., and logic circuit area (logic blocks) 231 are mounted on the same semiconductor chip.

In the logic block on the LSI chip 1 shown in FIG. 11, the gate array basic cells GC are arranged in the empty spaces of the standard cells SC while using channelless standard cells as the basic elements. In the prior art, the pattern arrangement of similar mixed type LSI chip which is called as the embedded array have been known. However, since either the gate array basic cells or the standard cells are spread all over the logic block in such embedded array, the underlying patterns must be changed or ion-implantation, etc. must be executed again if the circuit change is needed. As a consequence, a long period of time has been required to design and manufacture the circuit.

In the second embodiment of the present invention, as shown in FIG. 11, the gate array basic cells GC are arranged preliminarily in the empty spaces in which the standard cells SC are not arranged in the logic block 231, and the circuit change is made by use of the basic cells GC. Therefore, various circuit change can be implemented only by changing the wirings with no influence on the circuit configuration of the standard cells, so that turn around time can be shortened. In addition, if specifications of the standard cells SC and the basic cells GC are mated with each other to be arranged on the same grid, mixed standard cell and basic cell layout can be facilitated and also constraints in arrangement and routing can be relaxed widely in contrast to the prior art.

Especially, the gate array basic cells have such a disadvantage that sometimes power consumption cannot be reduced by reducing the transistors according to specifications since sizes of the transistors are fixed. In contrast, since sizes of the transistors can be varied even if the height of the cell is fixed, power consumption in the standard cells can be reduced by reducing the sizes of the transistors according to requested specifications. Hence, power consumption of overall LSI chip can be reduced by combining the gate array basic cells with the standard cells appropriately. Furthermore, it is similar to the first embodiment that intermediate buffers can be arranged easily by means of combinations of the standard cells and the gate array basic cells to increase the driving capability and to suppress the clock skew.

In the second embodiment of the present invention, it is a matter of course that the structure which has the wiring channel regions explained in the first embodiment may be adopted as patterns in the logic block 231. Of course, the structures explained in the first to sixth example of the first embodiment may be applied to the second embodiment.

Whether a total occupied area of the standard cells SC in the logic block 231 or the gate array basic cells GC is set larger is a matter of choice. A ratio of total areas may be selected depending upon circuit specifications.

Various modifications will become possible for those skilled in the art after receiving the teachings of the present disclosure without departing from the scope thereof.

What is claimed is:

1. A semicustom integrated circuit comprising:

(a) a plurality of cell rows, in each row a plurality of standard cell are arranged, the standard cells being configured as rectangular pattern regions having a predetermined height, and different widths so that the standard cells include first and second type cells; and

(b) gate array basic cells formed in an empty space of a predetermined cell row of the plurality of cells rows, each of the basic cells being configured as a rectangular pattern region having a height substantially identical to said predetermined height and a width equal to the width of the first type cell, said width of the basic cells not being equal to the width of the second type cell.

2. The integrated circuit of claim 1, wherein the basic cells are used to construct additional circuits for increasing driving capability to drive signals transmitted to a plurality of circuits disposed on a semiconductor substrate.

3. The integrated circuit of claim 1, further comprising; gate array basic cells formed in wiring channel regions disposed between the plurality of cell rows.

4. The integrated circuit of claim 1, wherein respective cell rows are arranged adjacently.

5. The integrated circuit of claim 3, wherein the basic calls formed in the wiring channel regions are formed on a basis of a rectangular pattern having a height substantially identical to that of the standard cells.

6. The integrated circuit of claim 3, wherein the standard cells and the basic cells are arranged adjacently along a direction orthogonal to the cell rows.

7. The integrated circuit of claim 4, wherein the standard cells and the basic cells are arranged adjacently along a direction orthogonal to the cell rows.

8. The integrated circuit of claim 3, wherein the standard cells and the basic cells which are arranged adjacently along a direction orthogonal to the cell rows have common signal lines.

9. The integrated circuit of claim 4, wherein the standard cells and the basic cells which are arranged adjacently along a direction orthogonal to the cell rows have common signal lines.

10. The integrated circuit of claim 1, wherein the standard cells and the basic cells have common power supply lines arranged along a straight line.

11. The integrated circuit of claim 1, wherein the standard cells and the basic cells have common signal lines arranged along a straight line.

12. The integrated circuit of claim 1, wherein widths of the standard cells are integral multiple of a width of the basic cells.

13. The integrated circuit of claim 5, wherein widths of the standard cells are integral multiple of a width of the basic cells.

14. The integrated circuit of claim 1, wherein the standard cells and the basic cells are arranged pursuant to a same grid system.

15. The integrated circuit of claim 3, wherein the standard cells and the basic cells are arranged pursuant to a same grid system.

16. The integrated circuit of claim 1, wherein the basic cells are used to construct intermediate buffers for distributing a clock signal to a plurality of circuits which are displaced on a semiconductor substrate.

17. The integrated circuit of claim 3, wherein the basic cells are used to construct intermediate buffers for distrib-

uting a clock signal to a plurality of circuits which are displaced on a semiconductor substrate.

18. The integrated circuit of claim **3**, wherein the basic cells are used to construct additional circuits for increasing driving capability to drive signals transmitted to a plurality of circuits disposed on a semiconductor substrate.

19. A semicustom integrated circuit having a logic circuit area and at least one of megacell and megafunction on a single semiconductor chip, the logic circuit area comprising:

(a) a plurality of cell rows, in each row a plurality of standard cells are arranged, the standard cells being configured as rectangular pattern regions having a predetermined height, and different widths so that the standard cells include first and second type cells; and

(b) gate array basic cells formed in an empty space of the standard cells in predetermined cell row of the plurality of cell rows, each of the basic cells being configured as a rectangular pattern region having a height substantially identical to said predetermined height and a width equal to the width of the first type cell, said width of the basic cells not being equal to the width of the second type cell.

20. The integrated circuit of claim **19**, further comprising:

gate array basic cells formed in wiring channel regions between the plurality of cell rows.

21. The integrated circuit of claim **10**, wherein the standard cells and the basic cells are arranged pursuant to a same grid system.

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